

Structure : Silicon Monolithic Integrated Circuit

Product name : Wide Bandwidth Audio-Video SW for TV

Type : **BH7645KS2**

Outer dimensions : Fig.1 SQFP-T52

Block diagram : Fig.2

- Features :
- 1) Video inputs selector : 2-inputs component, 2-inputs Y/C, and 2-inputs composite
 - 2) Component inputs : Correspond to D5 standard
 - 3) Built-in LPF selector(6.75MHz/13.5MHz/30MHz/Through)
 - 4) Built-in Video MUTE function
 - 5) Audio inputs selector : 6-inputs (Lch, Rch)
 - 6) Built-in Power-on MUTE function
 - 7) I²C-BUS control
 - 8) Optional Slave address modifications(90H/92H)
 - 9) I²C-BUS is compatible with fast mode of Version2.0, but not compatible with Hs mode
 - 10) Built-in detector 3ch(S_SW1/S_SW2/S_SW3)
 - 11) Built-in output port 2ch(PORT1_OUT/PORT2_OUT)

○ Absolute Maximum Ratings (Ta=+25°C)

Parameter		Symbol	Ratings	Unit
Supply voltage1 (2pin, 29pin, 33pin, 39pin, 44pin)		Vcc1	7	V
Supply voltage2 (12pin)		Vcc2	8.8	V
Power dissipation		Pd	1300 *1	mW
Input voltage range	VIDEO PART, LOGIC PART	V _{IN1}	0 ~ Vcc1+0.2	V
	AUDIO PART	V _{IN2}	0 ~ Vcc2+0.2	V
Storage temperature range		Tstg	-55 ~ +125	°C

*1 When mounting on a 70mm × 70mm × 1.6mm PCB board

Reduced by 13mW/°C at Ta = +25°C or higher

○ Operating Range

Parameter	Symbol	Range	Unit
Supply voltage1 (2pin, 29pin, 33pin, 39pin, 44pin)	Vcc1	+4.5 ~ +5.5	V
Supply voltage2 (12pin)	Vcc2	+7.5 ~ +8.5	V
Operating temperature range	Topr	-40 ~ +85	°C

* This product is not designed for protection against radioactive rays.

* Note the power supply sequence.

○Electrical characteristics (Unless otherwise specified, Ta= 25°C, Vcc1=5.0V, Vcc2=8.0V)

Item	Symbol	Limits			Unit	Conditions	
		Min.	Typ.	Max.			
[VIDEO PART]							
Circuit current	ICC _V	—	55	80	mA	No signal	
Voltage gain	GV _V	-0.5	0.0	0.5	dB	Vin=1.0Vpp, f=100kHz	
Frequency characteristics1 [f=6.75MHz LPF MODE]	GF _{1-1V}	-1.5	0.0	1.0	dB	Vin=1.0Vpp, f=6.75MHz/100kHz	
	GF _{1-2V}	—	-30	-20	dB	Vin=1.0Vpp, f=27MHz/100kHz	
Frequency characteristics 2 [f=13.5MHz LPF MODE]	GF _{2-1V}	-1.5	0.0	1.0	dB	Vin=1.0Vpp, f=13.5MHz/100kHz	
	GF _{2-2V}	—	-30	-20	dB	Vin=1.0Vpp, f=54MHz/100kHz	
Frequency characteristics 3 [f=30MHz LPF MODE]	GF _{3-1V}	-1.5	0.0	1.0	dB	Vin=1.0Vpp, f=30MHz/100kHz	
	GF _{3-2V}	—	-18	-10	dB	Vin=1.0Vpp, f=74MHz/100kHz	
Frequency characteristics 4 [f=THROUGH MODE]	GF _{4-1V}	-3.0	-0.5	2.0	dB	Vin=1.0Vpp, f=54MHz/100kHz	
Maximum output level	VOM _V	2.6	3.0	—	Vpp	f=10kHz, THD=1.0%	
SW crosstalk	CTSW _V	—	-60	-50	dB	Vin=1.0Vpp, f=10MHz	
Channel crosstalk	CTCH _V	—	-60	-50	dB	Vin=1.0Vpp, f=10MHz	
MUTE attenuation	MT _V	—	-60	-50	dB	Vin=1.0Vpp, f=10MHz	
Bias input terminal Input impedance	ZIN _V	100	150	—	kΩ		
[AUDIO PART] (at Gain=0dB)							
Circuit current	ICC _A	—	10	15	mA	No signal	
Voltage gain	0dB	GV0 _A	-0.5	0.0	0.5	dB	
	6dB	GV6 _A	5.5	6.0	6.5	dB	
Frequency characteristics	GF _A	-3.0	0.0	3.0	dB	Vin=1.0Vrms, f=50kHz/1kHz	
Total harmonic distortion	THD _A	—	0.03	0.1	%	Vin=1.0Vrms, f=1kHz ≈1	
Maximum output level	0dB	VOM0 _A	2.0	2.4	—	Vrms	
	6dB	VOM6 _A	2.0	2.4	—	Vrms	
Channel crosstalk	CTCH _A	—	-100	-85	dB	Vin=2.0Vrms, f=1kHz ≈1	
SW crosstalk	CTSW _A	—	-100	-85	dB	Vin=2.0Vrms, f=1kHz ≈1	
MUTE attenuation	MT _A	—	-100	-85	dB	Vin=2.0Vrms, f=1kHz ≈1	
Remain noise	N _A	—	30	50	uVrms	≈1	
PSRR	PSRR _A	—	-45	-38	dB	≈2	
Input impedance	ZIN _A	100	150	—	kΩ		
[LOGIC PART etc.]							
[SCL] [SDA]	VIL	Vin1L	0	—	1.0	V	Low Level input voltage
	VIH	Vin1H	2.0	—	Vcc1	V	High Level input voltage
	Input bias current	IINI2C	-10	0	10	uA	
	SDA output voltage	VinL	0	—	0.4	V	I _L =3.0mA(sink)
[ADR]	VIL	Vin2L	0	—	1.0	V	Low Level input voltage
	VIH	Vin2H	2.0	—	Vcc1	V	High Level input voltage
	Input impedance	ZIN _{ADR}	70	100	130	kΩ	
[S_SW1] [S_SW2] [S_SW3]	VIL	Vin2L	0	—	1.0	V	Low Level input voltage
	VIH	Vin2H	2.0	—	Vcc1	V	High Level input voltage
	Input impedance	ZIN _{SSW}	100	150	—	kΩ	Pull up resistance
[PORT1_OUT] [PORT2_OUT]	PORT output voltage	V _{PL}	—	—	0.5	V	I _L =2.5mA
	Leak current	I _{PH}	—	—	5.0	uA	Vcc2=8.0V

≈1 400HzHPF + 30kHzLPF ON

≈2 Vin=0.3Vpp, f=100Hz at VCC, 30kHzLPF ON

○Physical dimensions

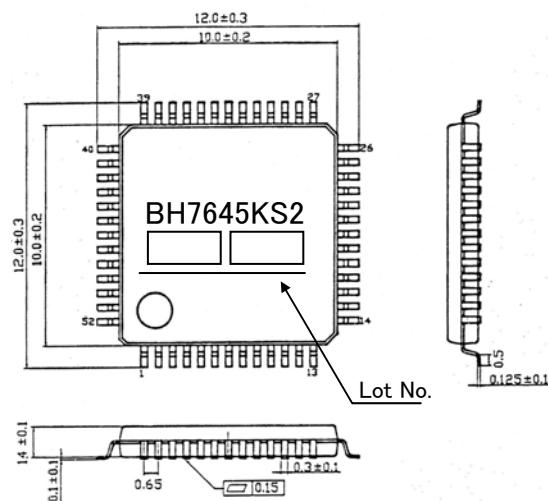


Fig.1 SQFP-T52 (UNIT:mm)

○Block diagram

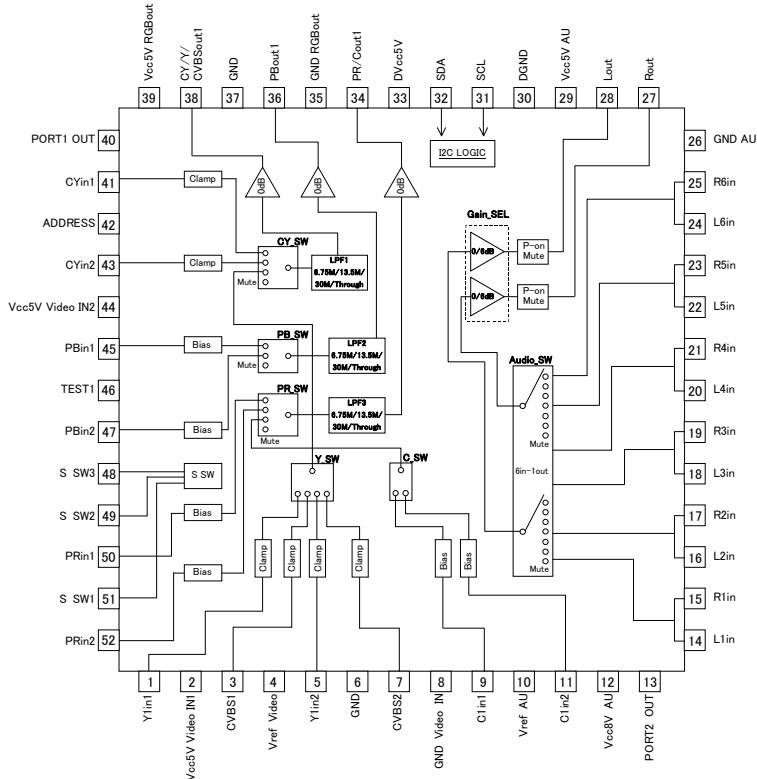


Fig.2 Block diagram

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	Y1in1	14	L1in	27	Rout	40	PORT1 OUT
2	Vcc5V Video IN1	15	R1in	28	Lout	41	CYin1
3	CVBS1	16	L2in	29	Vcc5V AU	42	ADDRESS
4	Vref Video	17	R2in	30	DGND	43	CYin2
5	Y1in2	18	L3in	31	SCL	44	Vcc5V Video IN2
6	GND	19	R3in	32	SDA	45	PBin1
7	CVBS2	20	L4in	33	DVcc5V	46	TEST1
8	GND Video IN	21	R4in	34	PR/Cout1	47	PBin2
9	C1in1	22	L5in	35	GND RGBout	48	S SW3
10	Vref AU	23	R5in	36	PBout1	49	S SW2
11	C1in2	24	L6in	37	GND	50	PRin1
12	Vcc8V AU	25	R6in	38	CY/Y/CVBSout1	51	S SW1
13	PORT2 OUT	26	GND AU	39	Vcc5V RGBout	52	PRin2

○Pin number and Pin name

○Cautions for use

(1) Absolute maximum ratings

If the absolute maximum ratings for applied voltage and/or operation temperature are exceeded, LSI damage may result. Therefore, do not apply voltage or use in a temperature that exceeds these absolute maximum ratings. If it is possible that absolute maximum ratings will be exceeded, use a physical safety device such as a fuse and make sure that no conditions that might exceed the absolute maximum ratings will be applied to the LSI IC.

(2) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND potential

Regardless of the operation mode, the voltage of the GND pin should be at least the minimum voltage. Actually check whether or not the voltage at each pin, including transient phenomena, is less than the GND pin voltage.

(4) Thermal design

The thermal design should be done using an ample margin that takes into consideration the allowable dissipation under actual use conditions.

(5) Shorts between pins and mounting errors

When mounting LSI ICs onto the circuit board, make sure each LSI's orientation and position is correct. The ICs may become damaged if they are not mounted correctly when the power is turned on. Similarly, damage may also result if a short occurs, such as when a foreign object is positioned between pins in an IC, or between a pin and a power supply or GND connection.

(6) Operation in strong electromagnetic field

When used within a strong electromagnetic field, evaluate carefully to avoid the risk of operation faults.

(7) Power supply sequence

[Power-up sequence]

Supply voltage1 (Vcc1 : 2pin, 29pin, 33pin, 39pin, 44pin) must be powered up before or at the same time as the supply voltage2 (Vcc2 : 12pin).

[Power-down sequence]

Supply voltage2 (Vcc2 : 12pin) must be powered up before or at the same time as the supply voltage1(Vcc1 : 2pin, 29pin, 33pin, 39pin, 44pin).

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